

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Chun-Chi WANG et al.

Serial No. 09/824,014

Filed: April 3, 2001

: EXPEDITED PROCEDURE
: Response under 37 CFR 1.116

: Group Art Unit: 2823

: Examiner: S. Foong

For: METHOD OF FORMING SHALLOW TRENCH ISOLATION STRUCTURE

BOX AF
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231Corres. and Mail
BOX AF

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☒ No additional fee is required.☐ Small entity status of this application has been established.☐ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	13	20	0	x \$ 18 =	
Independent Claims	3	3	0	x \$ 84 =	
If multiple claims newly presented, add \$280.00					
Fee for extension of time					
TOTAL FEE DUE					

☐ A credit card authorization form in the amount of is attached☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 07-1337, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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BJH/lcw



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: Suk-San FOONG
Group Art Unit: 2823

#5/B
V. Brown
4/24/03

In re PATENT APPLICATION of

Applicants: WANG ET AL.

Appl. No.: 09/824,014

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TECHNOLOGY CENTER 2800

AMENDMENT UNDER 37 CFR 1.116

Washington, D.C. 20231
Assistant Commissioner for Patents

Dear Sir:

In response to the Final Office Action dated January 8, 2003, please amend the application as follows:

IN THE SPECIFICATION:

Please amend the paragraph beginning on line 10, page 4, and carrying over onto page 5, as follows:

For at least the foregoing aspects discussed above, the present invention provides a method of forming the shallow trench isolation structure. While forming the shallow trench isolation structure in the integrated circuits, the method of the present invention etches the oxide layer on the first silicon nitride layer of the active area by the wet etching until the first silicon nitride layer is about exposed. Then, the second silicon nitride layer is deposited, and subsequently a photoresist is formed on the second silicon nitride layer to cover the whole shallow trench area. Portions of the second silicon nitride